

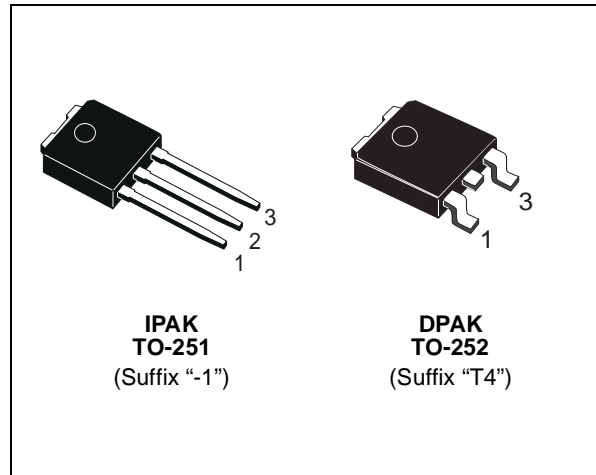


STD60NH03L

N-CHANNEL 30V - 0.0075 Ω - 60A DPAK/IPAK STripFET™ III POWER MOSFET

| TYPE | V _{DSS} | R _{DS(on)} | I _D |
|------------|------------------|---------------------|----------------|
| STD60NH03L | 30 V | < 0.009 Ω | 60 A |

- TYPICAL R_{DS(on)} = 0.0075 Ω @ 10 V
- TYPICAL R_{DS(on)} = 0.009 Ω @ 5 V
- R_{DS(on)} * Q_g INDUSTRY'S BENCHMARK
- CONDUCTION LOSSES REDUCED
- SWITCHING LOSSES REDUCED
- LOW THRESHOLD DEVICE
- THROUGH-HOLE IPAK (TO-251) POWER PACKAGE IN TUBE (SUFFIX "-1")
- SURFACE-MOUNTING DPAK (TO-252) POWER PACKAGE IN TAPE & REEL (SUFFIX "T4")



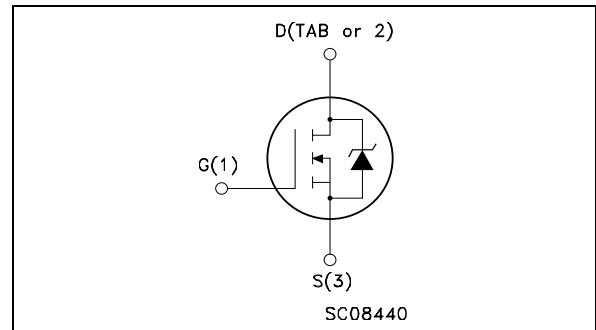
DESCRIPTION

The STD60NH03L utilizes the latest advanced design rules of ST's proprietary STripFET™ technology. This is suitable for the most demanding DC-DC converter application where high efficiency is to be achieved.

APPLICATIONS

- SPECIFICALLY DESIGNED AND OPTIMISED FOR HIGH EFFICIENCY DC/DC CONVERTERS

INTERNAL SCHEMATIC DIAGRAM



Ordering Information

| SALES TYPE | MARKING | PACKAGE | PACKAGING |
|--------------|----------|---------|-------------|
| STD60NH03LT4 | D60NH03L | TO-252 | TAPE & REEL |
| STD60NH03L-1 | D60NH03L | TO-251 | TUBE |

ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|----------------------------------|--|------------|------|
| V _{DS} | Drain-source Voltage (V _{GS} = 0) | 30 | V |
| V _{DGR} | Drain-gate Voltage (R _{GS} = 20 kΩ) | 30 | V |
| V _{GS} | Gate- source Voltage | ± 20 | V |
| I _D | Drain Current (continuous) at T _C = 25°C | 60 | A |
| I _D | Drain Current (continuous) at T _C = 100°C | 43 | A |
| I _{DM} (¹) | Drain Current (pulsed) | 240 | A |
| P _{tot} | Total Dissipation at T _C = 25°C | 70 | W |
| | Derating Factor | 0.47 | W/°C |
| E _{AS} (²) | Single Pulse Avalanche Energy | 300 | mJ |
| T _{stg} | Storage Temperature | -55 to 175 | °C |
| T _j | Max. Operating Junction Temperature | | |

STD60NH03L

THERMAL DATA

| | | | | |
|----------------|--|-----|------|------|
| Rthj-case | Thermal Resistance Junction-case | Max | 2.14 | °C/W |
| Rthj-amb | Thermal Resistance Junction-ambient | Max | 100 | °C/W |
| Rthj-pcb | Thermal Resistance Junction-pcb(#) | Max | 43 | °C/W |
| T _l | Maximum Lead Temperature For Soldering Purpose | | 275 | °C |

(#) When Mounted on 1 inch² FR-4 board, 2 oz of Cu.

ELECTRICAL CHARACTERISTICS (T_{CASE} = 25 °C UNLESS OTHERWISE SPECIFIED)

OFF

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|----------------------|---|---|------|------|---------|----------|
| V _{(BR)DSS} | Drain-source Breakdown Voltage | I _D = 250 μA, V _{GS} = 0 | 30 | | | V |
| I _{DSS} | Zero Gate Voltage Drain Current (V _{GS} = 0) | V _{DS} = Max Rating V _{DS} = Max Rating T _C = 125°C | | | 1 10 | μA μA |
| I _{GSS} | Gate-body Leakage Current (V _{DS} = 0) | V _{GS} = ± 20V | | | ±100 | nA |

ON (4)

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---------------------|-----------------------------------|---|------|-----------------|----------------|--------|
| V _{GS(th)} | Gate Threshold Voltage | V _{DS} = V _{GS} I _D = 250 μA | 1 | | | V |
| R _{DS(on)} | Static Drain-source On Resistance | V _{GS} = 10 V I _D = 30 A V _{GS} = 5 V I _D = 30 A | | 0.0075 0.009 | 0.009 0.017 | Ω Ω |

DYNAMIC

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|--|---|---|------|-------------------|------|----------------|
| g _{fs} (4) | Forward Transconductance | V _{DS} = 15 V I _D = 18 A | | 25 | | S |
| C _{iss} C _{oss} C _{rss} | Input Capacitance Output Capacitance Reverse Transfer Capacitance | V _{DS} = 10V f = 1 MHz V _{GS} = 0 | | 2200 380 49 | | pF pF pF |
| R _G | Gate Input Resistance | f = 1 MHz Gate DC Bias = 0 Test Signal Level = 20 mV Open Drain | | 1.5 | | Ω |

ELECTRICAL CHARACTERISTICS (continued)

SWITCHING ON

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|-------------------------------|--|---|------|--------------------|------|----------------|
| $t_{d(on)}$ t_r | Turn-on Delay Time Rise Time | $V_{DD} = 15\text{ V}$ $I_D = 30\text{ A}$ $R_G = 4.7\ \Omega$ $V_{GS} = 5\text{ V}$ (Resistive Load, Figure 3) | | 21 95 | | ns ns |
| Q_g Q_{gs} Q_{gd} | Total Gate Charge Gate-Source Charge Gate-Drain Charge | $V_{DD} = 15\text{ V}$ $I_D = 60\text{ A}$ $V_{GS} = 5\text{ V}$ | | 15.7 8.3 3.4 | 21 | nC nC nC |
| $Q_{gls}^{(4)}$ | Third-quadrant Gate Charge | $V_{DS} < 0\text{ V}$ $V_{GS} = 10\text{ V}$ | | 15 | | nC |

SWITCHING OFF

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|-----------------------|----------------------------------|---|------|----------|------|----------|
| $t_{d(off)}$ t_f | Turn-off Delay Time Fall Time | $V_{DD} = 15\text{ V}$ $I_D = 30\text{ A}$ $R_G = 4.7\ \Omega$, $V_{GS} = 5\text{ V}$ (Resistive Load, Figure 3) | | 19 15 | | ns ns |

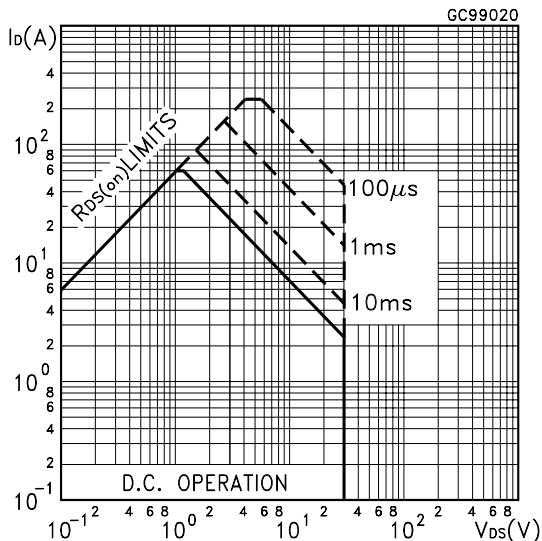
SOURCE DRAIN DIODE

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|-----------------------------------|--|---|------|-----------------|-----------|---------------|
| I_{SD} I_{SDM} | Source-drain Current Source-drain Current (pulsed) | | | | 60 240 | A A |
| V_{SD} | Forward On Voltage | $I_{SD} = 30\text{ A}$ $V_{GS} = 0$ | | | 1.4 | V |
| t_{rr} Q_{rr} I_{RRM} | Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current | $I_{SD} = 60\text{ A}$ $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 20\text{ V}$ $T_j = 150^\circ\text{C}$ (see test circuit, Figure 5) | | 32 51 3.2 | | ns nC A |

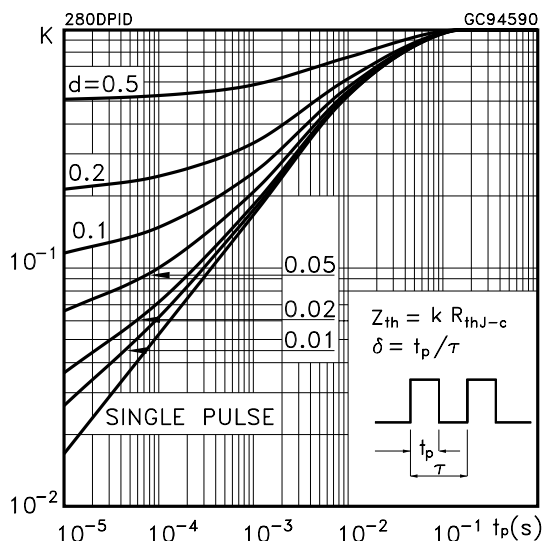
(1) Pulse width limited by safe operating area
(2) Starting $T_j = 25^\circ\text{C}$, $I_D = 30\text{ A}$, $V_{DD} = 20\text{ V}$

(3) Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %
(4) Gate charge for synchronous operation. See Appendix A

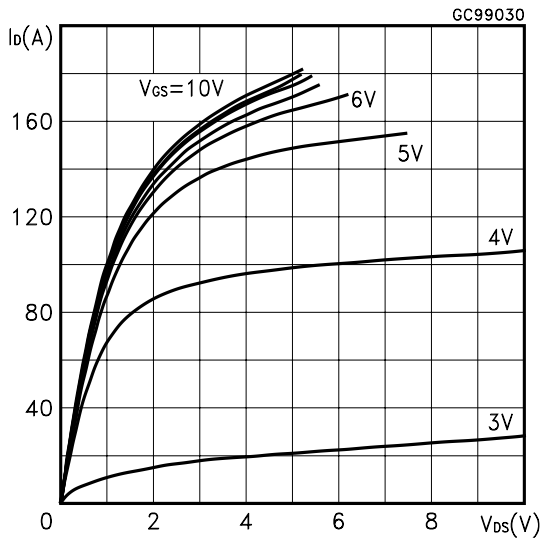
Safe Operating Area



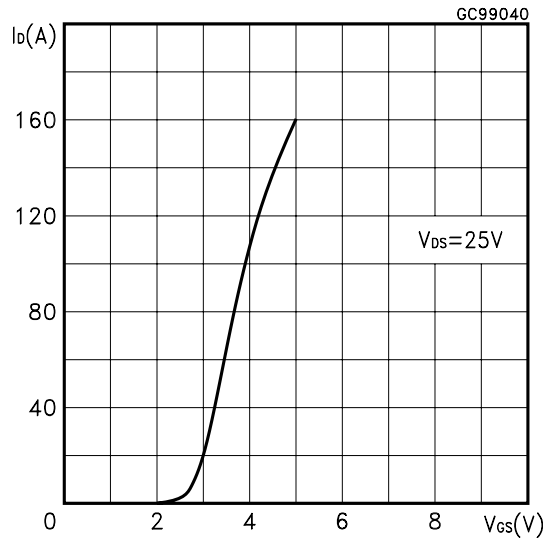
Thermal Impedance



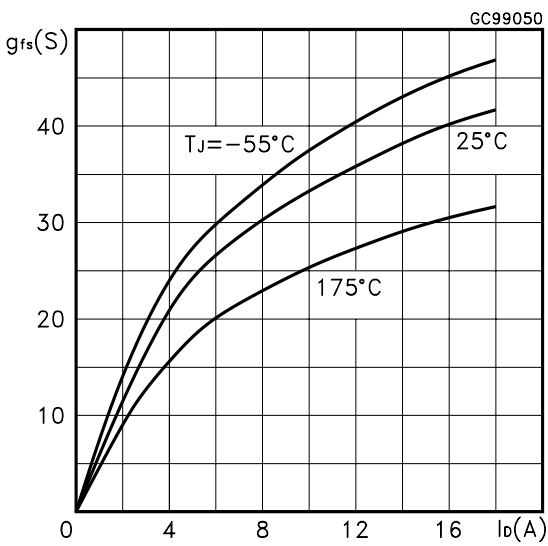
Output Characteristics



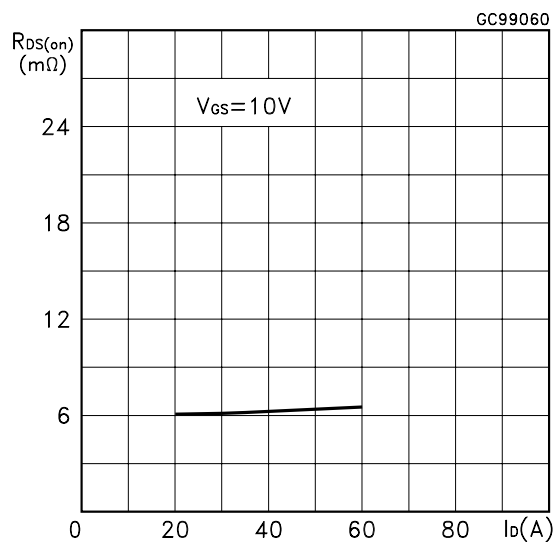
Transfer Characteristics



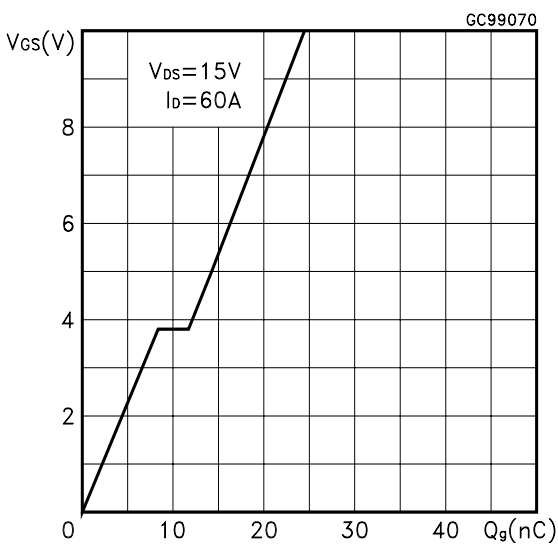
Transconductance



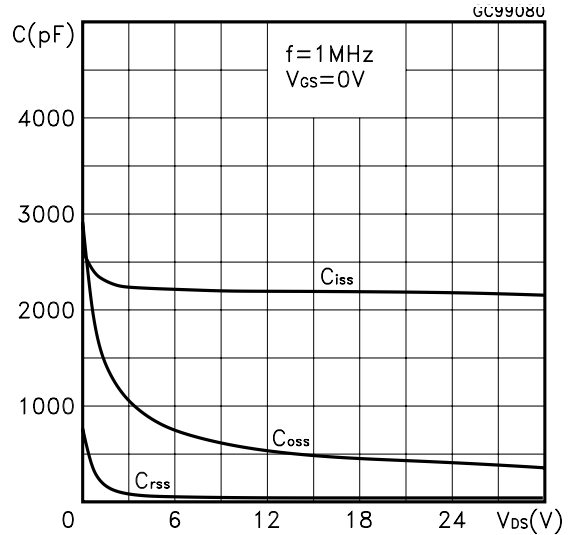
Static Drain-source On Resistance



Gate Charge vs Gate-source Voltage

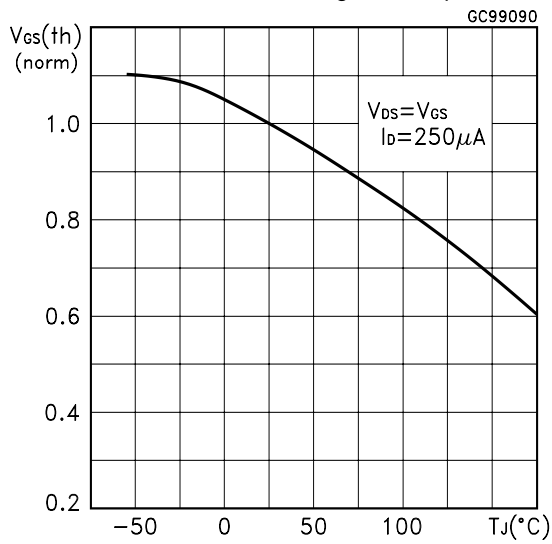


Capacitance Variations

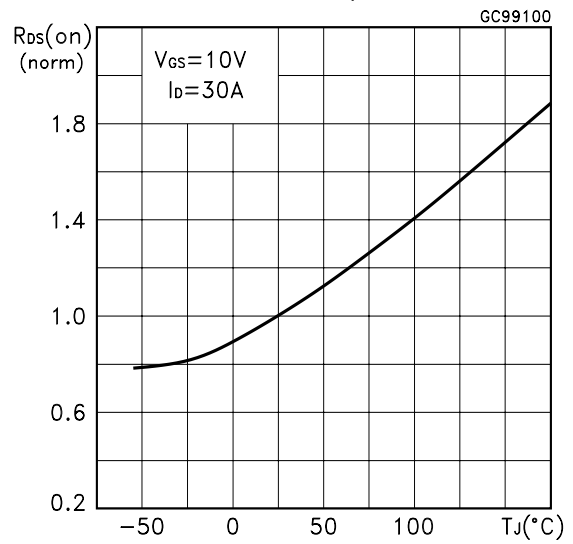


STD60NH03L

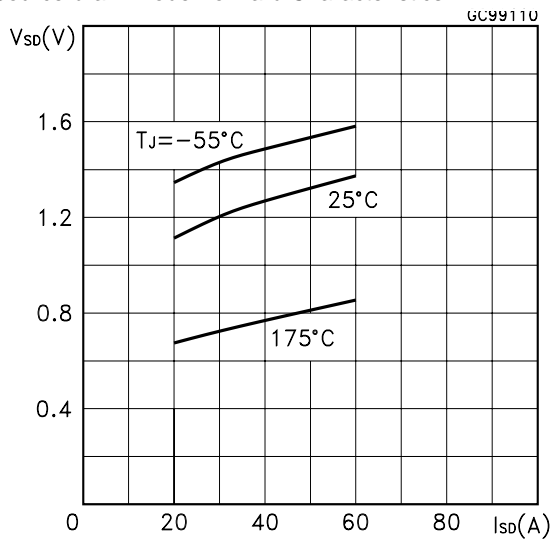
Normalized Gate Threshold Voltage vs Temperature



Normalized on Resistance vs Temperature



Source-drain Diode Forward Characteristics



Normalized Breakdown Voltage vs Temperature

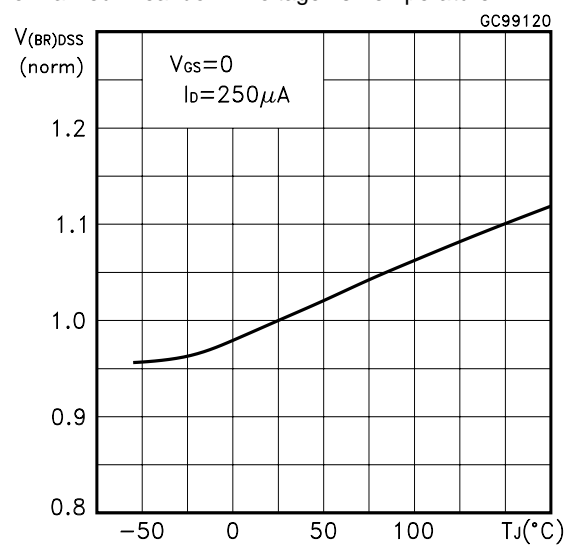


Fig. 1: Unclamped Inductive Load Test Circuit

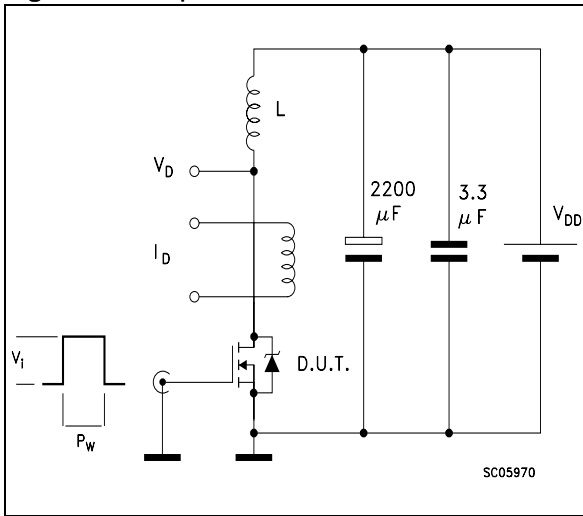


Fig. 2: Unclamped Inductive Waveform

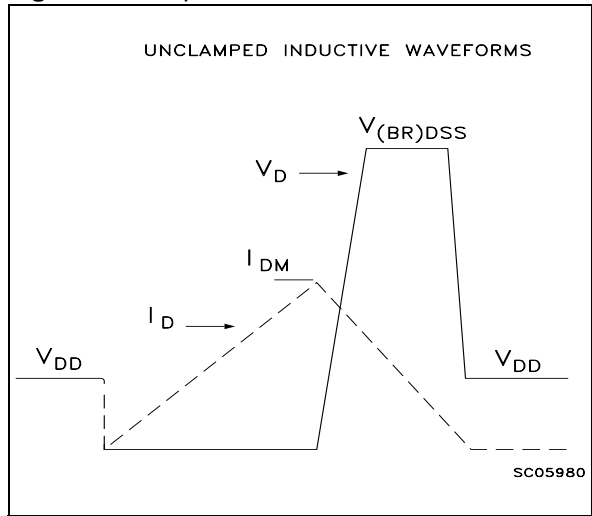


Fig. 3: Switching Times Test Circuits For Resistive Load

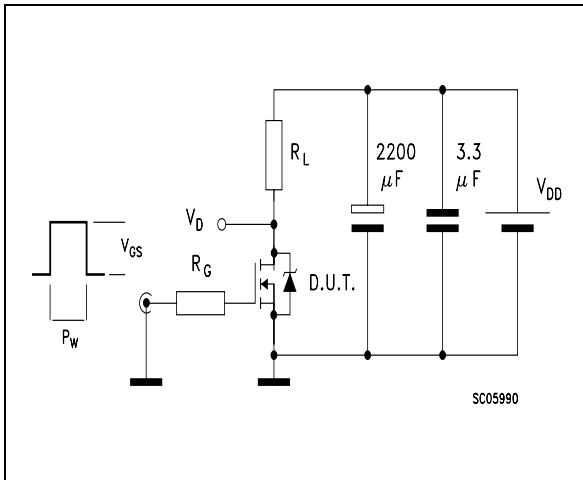


Fig. 4: Gate Charge test Circuit

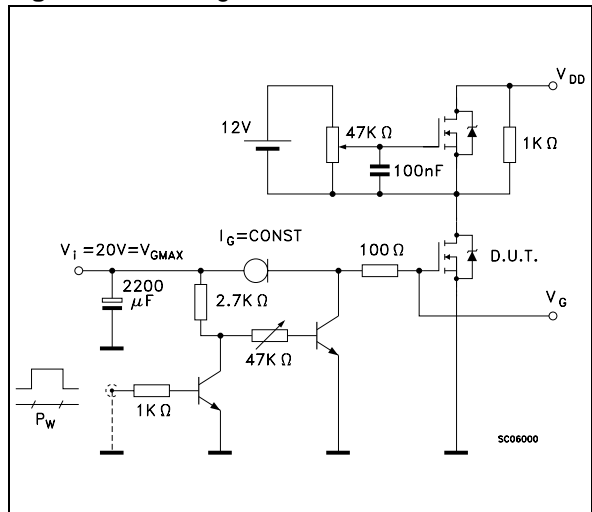
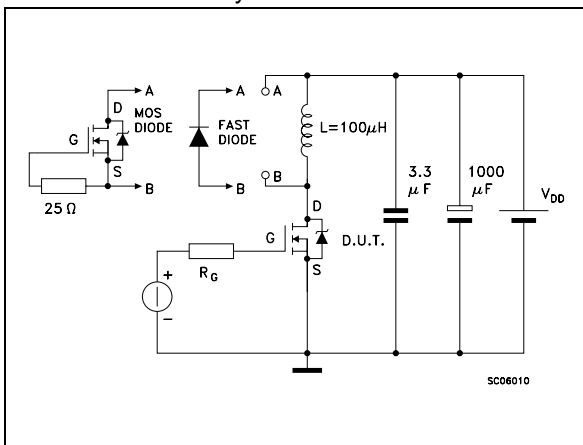
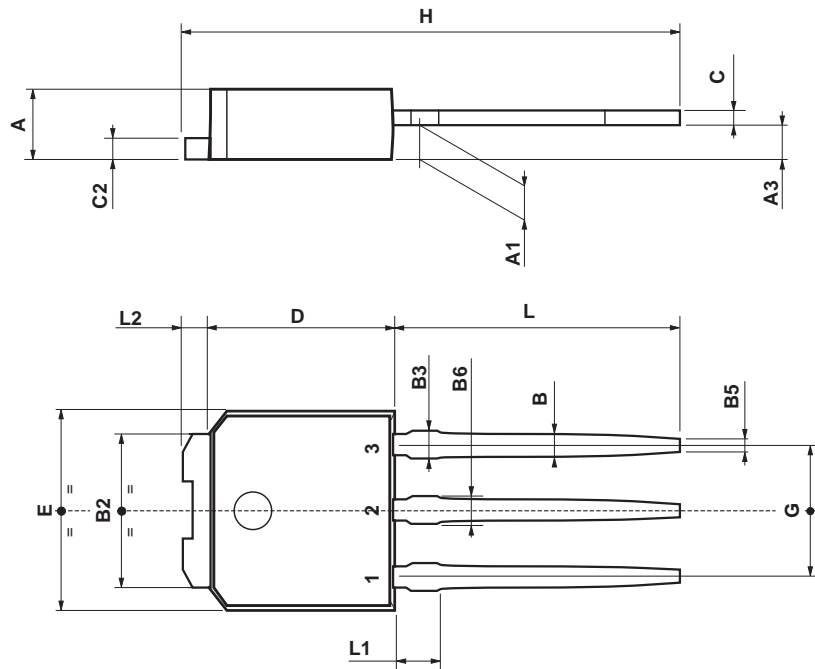


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



TO-251 (IPAK) MECHANICAL DATA

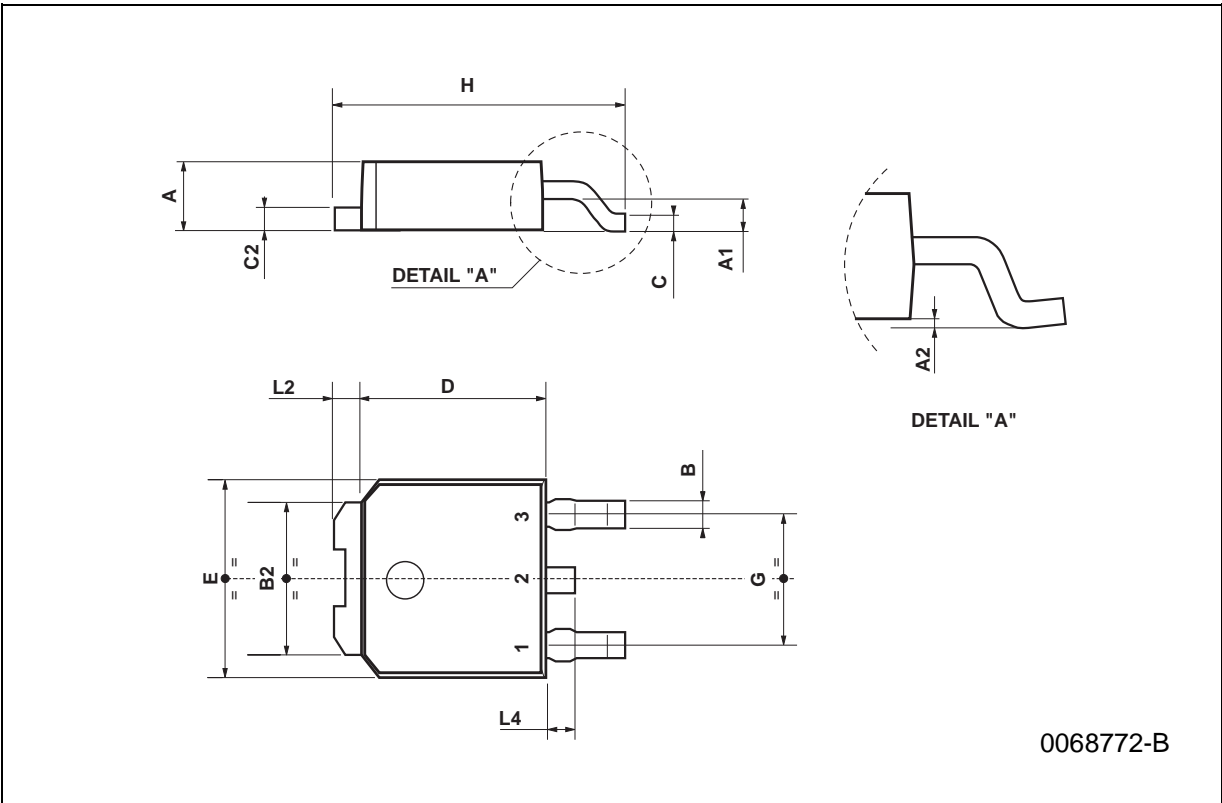
| DIM. | mm | | | inch | | |
|------|------|------|------|-------|-------|-------|
| | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. |
| A | 2.2 | | 2.4 | 0.086 | | 0.094 |
| A1 | 0.9 | | 1.1 | 0.035 | | 0.043 |
| A3 | 0.7 | | 1.3 | 0.027 | | 0.051 |
| B | 0.64 | | 0.9 | 0.025 | | 0.031 |
| B2 | 5.2 | | 5.4 | 0.204 | | 0.212 |
| B3 | | | 0.85 | | | 0.033 |
| B5 | | 0.3 | | | 0.012 | |
| B6 | | | 0.95 | | | 0.037 |
| C | 0.45 | | 0.6 | 0.017 | | 0.023 |
| C2 | 0.48 | | 0.6 | 0.019 | | 0.023 |
| D | 6 | | 6.2 | 0.236 | | 0.244 |
| E | 6.4 | | 6.6 | 0.252 | | 0.260 |
| G | 4.4 | | 4.6 | 0.173 | | 0.181 |
| H | 15.9 | | 16.3 | 0.626 | | 0.641 |
| L | 9 | | 9.4 | 0.354 | | 0.370 |
| L1 | 0.8 | | 1.2 | 0.031 | | 0.047 |
| L2 | | 0.8 | 1 | | 0.031 | 0.039 |



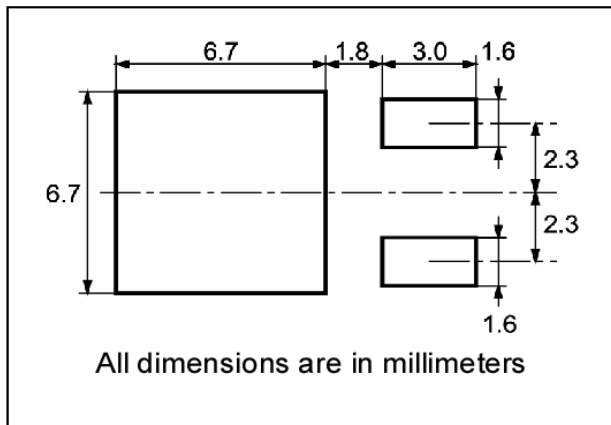
0068771-E

TO-252 (DPAK) MECHANICAL DATA

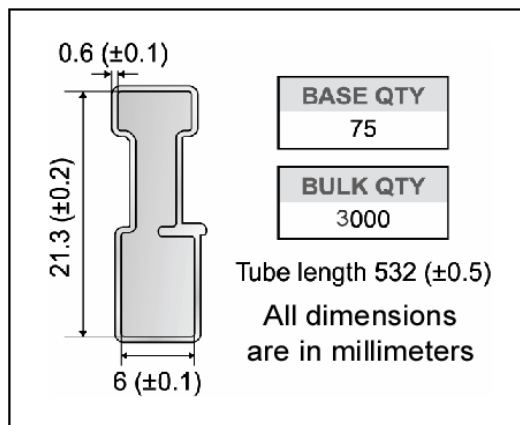
| DIM. | mm | | | inch | | |
|------|------|------|------|-------|-------|-------|
| | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. |
| A | 2.2 | | 2.4 | 0.086 | | 0.094 |
| A1 | 0.9 | | 1.1 | 0.035 | | 0.043 |
| A2 | 0.03 | | 0.23 | 0.001 | | 0.009 |
| B | 0.64 | | 0.9 | 0.025 | | 0.035 |
| B2 | 5.2 | | 5.4 | 0.204 | | 0.212 |
| C | 0.45 | | 0.6 | 0.017 | | 0.023 |
| C2 | 0.48 | | 0.6 | 0.019 | | 0.023 |
| D | 6 | | 6.2 | 0.236 | | 0.244 |
| E | 6.4 | | 6.6 | 0.252 | | 0.260 |
| G | 4.4 | | 4.6 | 0.173 | | 0.181 |
| H | 9.35 | | 10.1 | 0.368 | | 0.397 |
| L2 | | 0.8 | | | 0.031 | |
| L4 | 0.6 | | 1 | 0.023 | | 0.039 |



DPAK FOOTPRINT



TUBE SHIPMENT (no suffix)*



TAPE AND REEL SHIPMENT (suffix "T4")*

40 mm min. Access hole at slot location

Full radius

Tape slot in core for tape start 2.5mm min. width

G measured at hub

REEL MECHANICAL DATA

| DIM. | mm | | inch | |
|------|------|------|-------|--------|
| | MIN. | MAX. | MIN. | MAX. |
| A | | 330 | | 12.992 |
| B | 1.5 | | 0.059 | |
| C | 12.8 | 13.2 | 0.504 | 0.520 |
| D | 20.2 | | 0.795 | |
| G | 16.4 | 18.4 | 0.645 | 0.724 |
| N | 50 | | 1.968 | |
| T | | 22.4 | | 0.881 |

| | |
|-----------------|------|
| BASE QTY | 1000 |
| BULK QTY | 1000 |

TAPE MECHANICAL DATA

| DIM. | mm | | inch | |
|------|------|------|-------|-------|
| | MIN. | MAX. | MIN. | MAX. |
| A0 | 6.8 | 7 | 0.267 | 0.275 |
| B0 | 10.4 | 10.6 | 0.409 | 0.417 |
| B1 | | 12.1 | | 0.476 |
| D | 1.5 | 1.6 | 0.059 | 0.063 |
| D1 | 1.5 | | 0.059 | |
| E | 1.65 | 1.85 | 0.065 | 0.073 |
| F | 7.4 | 7.6 | 0.291 | 0.299 |
| K0 | 2.55 | 2.75 | 0.100 | 0.108 |
| P0 | 3.9 | 4.1 | 0.153 | 0.161 |
| P1 | 7.9 | 8.1 | 0.311 | 0.319 |
| P2 | 1.9 | 2.1 | 0.075 | 0.082 |
| R | 40 | | 1.574 | |
| W | 15.7 | 16.3 | 0.618 | 0.641 |

For machine ref. only including draft and radii concentric around B0

10 pitches cumulative tolerance on tape + / - 0.2 mm

Center line of cavity

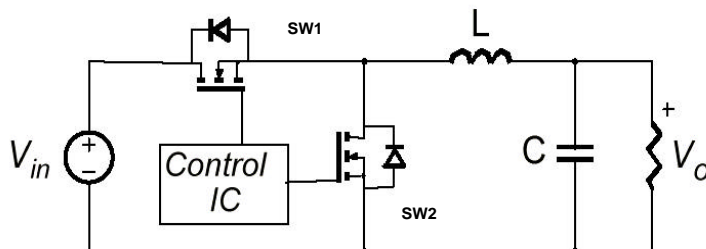
User Direction of Feed

FEED DIRECTION

Bending radius R min.

APPENDIX A

Buck Converter: Power Losses Estimation



The power losses associated with the FETs in a Synchronous Buck converter can be estimated using the equations shown in the table below. The formulas give a good approximation, for the sake of performance comparison, of how different pairs of devices affect the converter efficiency. However a very important parameter, the working temperature, is not considered. The real device behavior is really dependent on how the heat generated inside the devices is removed to allow for a safer working junction temperature.

The low side (SW2) device requires:

- Very low $R_{DS(on)}$ to reduce conduction losses
- Small Q_{gs} to reduce the gate charge losses
- Small C_{oss} to reduce losses due to output capacitance
- Small Q_{tr} to reduce losses on SW₁ during its turn-on
- The C_{gd}/C_{gs} ratio lower than V_{th}/V_{gg} ratio especially with low drain to source voltage to avoid the cross conduction phenomenon;

The high side (SW1) device requires:

- Small R_g and L_s to allow higher gate current peak and to limit the voltage feedback on the gate
- Small Q_g to have a faster commutation and to reduce gate charge losses
- Low $R_{DS(on)}$ to reduce the conduction losses.

| | | High Side Switch (SW1) | Low Side Switch (SW2) |
|------------------|------------|--|---------------------------------------|
| $P_{conduction}$ | | $R_{DS(on)SW1} * I_L^2 * d$ | $R_{DS(on)SW2} * I_L^2 * (1-d)$ |
| $P_{switching}$ | | $V_{in} * (Q_{gsth(SW1)} + Q_{gd(SW1)}) * f * \frac{I_L}{I_g}$ | Zero Voltage Switching |
| P_{diode} | Recovery | Not Applicable | $^1 V_{in} * Q_{rr(SW2)} * f$ |
| | Conduction | Not Applicable | $V_{r(SW2)} * I_L * t_{deadtime} * f$ |
| $P_{gate(Q_G)}$ | | $Q_{g(SW1)} * V_{gg} * f$ | $Q_{gls(SW2)} * V_{gg} * f$ |
| P_{Qoss} | | $\frac{V_{in} * Q_{oss(SW1)} * f}{2}$ | $\frac{V_{in} * Q_{oss(SW2)} * f}{2}$ |

| Parameter | Meaning |
|--------------------|--|
| d | Duty-cycle |
| Q_{gsth} | Post threshold gate charge |
| Q_{gls} | Third quadrant gate charge |
| Pconduction | On state losses |
| Pswitching | On-off transition losses |
| Pdiode | Conduction and reverse recovery diode losses |
| Pgate | Gate drive losses |
| PQoss | Output capacitance losses |

¹ Dissipated by SW1 during turn-on

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